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WHAT IS CLAIMED IS:

1. A liquid crystal display, comprising:

a liquid crystal panel including a plurality of gate lines, a plurality of data lines perpendicularly intersecting the gate lines, a plurality of liquid crystal capacitors coupled to a previous gate line and having liquid crystals between pixel electrodes and a common electrode, and a plurality of thin film transistors connected to the pixel electrodes of the liquid crystal capacitors;

a timing controller receiving image signals and synchronization signals, and generating control signals;

a gate driver sequentially applying a stepped-wave pattern gate voltage to a plurality of the gate lines, the stepped-wave pattern gate voltage including a first interval for converting a pixel grayscale level of a subsequent gate line formed in a previous frame to a first grayscale level, and a second interval for forming a path through which data voltage is applied by controlling the thin film transistors to on; and

a data driver for applying a data voltage of a second grayscale level supplied to the liquid crystal capacitors of the liquid crystal panel according to the control signals of the timing controller.

- 2. The liquid crystal display of claim 1, wherein the first grayscale level is a black grayscale level when in a normally white mode.
- 3. The liquid crystal display of claim 1, wherein the first grayscale level is a white grayscale level when in a normally black mode.
 - 4. The liquid crystal display of claim 1, wherein the gate voltage further

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includes a third interval for applying a voltage of the same polarity as the data voltage during a predetermined interval before the first interval and following the turning off of the thin film transistors.

5. A drive method for a liquid crystal display, the liquid crystal display including: a liquid crystal panel having a plurality of gate lines, a plurality of data lines perpendicularly intersecting the gate lines, a plurality of liquid crystal capacitors coupled to a previous gate line and having liquid crystals between pixel electrodes and a common electrode, and a plurality of thin film transistors connected to the pixel electrodes of the liquid crystal capacitors; a gate driver for generating a signal supplied to gates of the thin film transistors; and a data driver for generating a data voltage supplied to the liquid crystal capacitors of the liquid crystal panel, the method comprising the steps of:

sequentially applying a stepped-wave pattern gate voltage to the gate lines, the stepped-wave pattern gate voltage including a first interval for converting a pixel grayscale level of a subsequent gate line formed in a previous frame to a first grayscale level, and a second interval for forming a path through which data voltage is applied by controlling the thin film transistors to on; and

applying a data voltage charged in the liquid crystal capacitors to the liquid crystal panel.

6. The method of claim 5, wherein the gate voltage further includes a third interval for applying a voltage of the same polarity as the data voltage during a predetermined interval before the first interval and following the turning off of the thin film transistors.

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- 7. The method of claim 6, wherein the gate voltage in the first interval is identical in polarity to a polarity of the gate voltage in the third interval.
- 8. The method of claim 6, wherein the gate voltage in the first interval is opposite in polarity to a polarity of the gate voltage in the third interval.
- 9. The method of claim 6, wherein the gate voltage in the third interval is $\pm 3V$ to $\pm 10V$ relative to a gate-off voltage.
- 10. The method of claim 6, wherein the third interval starts at a point where the second interval ends, and converts to a gate-off voltage at a position where the second interval doubles.
- 11. The method of claim 5, wherein the first grayscale level is a white grayscale level when in a normally black mode.
- 12. The method of claim 5, wherein the first grayscale level is a black grayscale level when in a normally white mode.
- 13. The method of claim 5, wherein the gate voltage in the first interval is $\pm 3V$ to $\pm 10V$ relative to a gate-off voltage.
- 14. The method of claim 5, wherein a starting point of the first interval is within 0.5ms 5ms from a starting point of the second interval.